

What is claimed is:

- 1 1. A general purpose state machine comprising:
2 a first plurality of external input terminals for receiving information
3 from an external circuit;
4 a first multiplexer having a plurality of input terminals, at least some of
5 which are coupled to the external input terminals to receive the information therefrom, the
6 first multiplexer supplying a first output signal;
7 a programmable memory storing a plurality of words, each word
8 having a plurality of bits, a word from the memory being supplied in response to an address
9 signal;
10 a control circuit connected to receive the output signal from the first
11 multiplexer and connected to receive a first set of bits from a word in the programmable
12 memory, the control circuit providing a signal selecting one of the words in the
13 programmable memory; and
14 wherein the external circuit is connected to receive at least a second set
15 of bits from the same word of the programmable memory as the first set of bits in response to
16 selection of a word by the control circuit.
- 1 2. A general purpose state machine as in claim 1 further comprising a
2 decoder coupled between the control circuit and the programmable memory, wherein the
3 decoder is coupled to receive the signal from the control circuit, decode that signal, and
4 thereby provide the address signal to select the word to be supplied by the programmable
5 memory.
- 1 3. A general purpose state machine as in claim 2 further comprising a
2 register connected between the decoder and the control circuit to temporarily store the signal
3 from the control circuit selecting one of the words in the programmable memory.
- 1 4. A general purpose state machine as in claim 2 wherein the control
2 circuit is coupled to also receive as an input signal, an address of a word previously selected.
- 1 5. A general purpose state machine as in claim 1 wherein the first set of
2 bits received by the control circuit represents an address of a single word in the
3 programmable memory.

1 6. A general purpose state machine as in claim 5 wherein the signal from
2 the control circuit selects between the address provided by the first set of bits and the address
3 of the word previously selected.

1 7. A general purpose state machine as in claim 5 wherein the first set of
2 bits received by the control circuit represents addresses of two different words in the
3 programmable memory.

1 8. A general purpose state machine as in claim 7 wherein:
2 the control circuit is coupled to also receive as an input signal, an address of a
3 word previously selected; and
the control circuit selects among the two addresses represented by the first set
of bits and the address of the previously selected word.

1 9. A general purpose state machine as in claim 1 wherein the input
2 terminals of the first multiplexer are also connected to receive a third set of bits from the
3 programmable memory.

1 10. A general purpose state machine as in claim 9 further comprising a
2 second multiplexer having input terminals connected to each of the external input terminals,
3 connected to the programmable memory to receive a fourth set of bits therefrom, and
4 connected to provide an output signal to the control circuit.

1 11. A general purpose state machine as in claim 1 further comprising
2 programmable logic coupled to at least some of the external input terminals and coupled to
3 the first multiplexer to process information from the external circuit before it is provided to
4 the first multiplexer.

1 12. A general purpose state machine as in claim 11 wherein the
2 programmable logic comprises:
3 a first plurality of multiplexers connected in parallel to a plurality of external
4 input terminals to provide a corresponding first plurality of output lines, each of the first
5 plurality of multiplexers having a plurality of input terminals, each one of which is coupled to
6 one of a first potential source and a second potential source; and
7

8 a second plurality of multiplexers also connected in parallel to the plurality of
9 external input terminals to provide a corresponding second plurality of output lines, each of
10 the second plurality of multiplexers having a plurality of input terminals, each one of which is
11 coupled to one of the first potential source and the second potential source.

1 13. A general purpose state machine as in claim 1 further comprising at
2 least one counter coupled to at least some of the external input terminals and coupled to the
3 first multiplexer to process information from the external circuit before it is provided to the
4 first multiplexer.

1 14. A general purpose state machine as in claim 1 further comprising at
2 least one flag circuit coupled to at least some of the external input terminals and coupled to
3 the first multiplexer to process information from the external circuit before it is provided to
4 the first multiplexer.

1 15. A general purpose state machine as in claim 10 further comprising
2 programmable logic coupled to at least some of the external input terminals and coupled to
3 the second multiplexer to process information from the external circuit before it is provided
4 to the second multiplexer.

1 16. A general purpose state machine as in claim 14 further comprising at
2 least one counter coupled to at least some of the external input terminals and coupled to the
3 second multiplexer to process information from the external circuit before it is provided to
4 the second multiplexer.

1 17. A general purpose state machine as in claim 10 further comprising at
2 least one flag circuit coupled to at least some of the external input terminals and coupled to
3 the second multiplexer to process information from the external circuit before it is provided
4 to the second multiplexer.

1 18. A general purpose state machine comprising:
2 a programmable memory storing a plurality of words, each word having a
3 plurality of bits, a word from the memory being supplied in response to an address signal;
4 a control circuit coupled to receive at least first and second address signals
5 from a word in the programmable memory, and coupled to receive signals from an external

6 circuit, control circuit selecting one of the first address or the second address in response to
7 the signals from the external circuit; and
8 wherein by selection of one of the address signals, the control circuit
9 implements one of an unconditional branch operation or a two-way conditional branch
10 operation.

1 19. A general purpose state machine as in claim 17 wherein:
2 the control circuit is also coupled to receive a third address signal representing
3 a previously addressed word; and
4 by selection of one of the address signals, the control circuit implements one
5 of an unconditional branch operation, a two-way conditional branch operation, a three-way
6 conditional branch operation, or a wait until conditional branch operation.